X AND Ku BAND HIGH POWER GaAs FETs

Y.Yamada,H.Kuroda,H.Izumi,T.Soezima,
H.Wakamatsu and S.Hori

Microwave Solid-State Department
Komukai Works,Toshiba Corporation
Kawasaki,210,Japan

ABSTRACT

Internally matched GaAs FETs, with output powers of more than 10W,have been developed for the 10.7-11.7 and 14.0-14.5 GHz bands. These devices, with a total gate width of 32mm,consist of two chips that are fabricated by diect ion implantation and chemical dry etching. At 14.25 GHz,the Ku band device has achieved an output power of 41dBm,a power gain of 5 dB and a power added efficiency of 21 %. At 11.2 GHz,the X band device has delivered 41.2 dBm,5.8 dB and 25% respectively at the 1 dB gain compression point.

INTRODUCTION

In recent years,there has been an increase in the use of GaAs power FETs as substitutes for TWT amplifiers in X-band radar and microwave communication and Ku band satellite communication systems.Especially in X to Ku band, that is becoming the main frequency of microwave communication systems,GaAs power FETs with execellent performance,such as high power,high gain and high efficiency,have been in strong demand. In addition,the microwave communication systems also require FET amplifiers with small size and low cost(1)(2)(3).

In a high power device,multiple chips with large gate widths should be well combined by internal matching circuits. Therefore,chip-to-chip uniformity and low loss internal matching are necessary to increase the power-combining efficiency in the multichip device.

This paper descrives the several process techniques which help to improve chip uniformity and internal matching, and the performance results of 10W-power GaAs FETs for X to Ku band will be presented. These techniques involve direct ion implantation, chemical dry etching and an accurate wire bonding technique,by the use of an automatic bonder and an FET chip design suitable for bonding.

CHIP DESIGN

Fig.1 shows a photograph of the GaAs FET chip. A gate length of 0.5 μm and a finger length of 80 μm were chosen for X to Ku band operation. The gate pitch was 15 μm and the source-drain finger to finger spacing was 8 μm,in which ohmic contact regions (n+regions) were formed having 5 μm-spacing. The total gate width was set at 16 mm to obtain an output power of more than 6 W from a single chip. The chip size is 3.4 mm × 0.6 mm.

As seen in the photograph,the gate pad(along the top) and the drain pad(along the bottom) have long and slender patterns. In a multichip device in which each chip is individually matched with its own input and output circuits,differences in wire length frequently take place,due to displacement between the FET chip and the circuit elements to be mounted. Since this new pattern has no defined bonding pads,it is possible to determine the bond positions on the FET chip necessary to keep a fixed wire length.

Air bridges and via holes were used to reduce the parasitic capacitance and the inductance respectively. The FET chip was 30 μm thick,and a gold-plated heat sink(PHS) 50 μm thick was formed on its back.

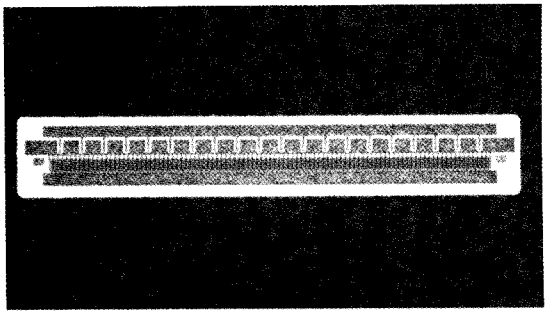

Fig.1 GaAs FET chip

0149-645X/88/0000-0847$01.00 © 1988 IEEE

FABRICATION PROCESS

The direct ion implantation technique was used to form active layers uniformly, across the 2-inch wafer. The Si^+ was implanted with energies of 70 KeV, and 200 KeV, and with respective doses of 1.5E12 cm^{-2}, and 4.8E12 cm^{-2}. The peak concentration and the depth of the active layers are about 1.7E17 cm^{-3} and 0.27 μm respectively. The source and drain electrodes were formed by alloying Pt/AuGe. The Al gates were defined by using the direct electron beam lithography and lift-off technique. The resulting variation in the gate electrodes is within ±0.06 μm for the length across the 2-inch wafer. The alignment accuracy is within ±0.1 μm.

The via hole structure and chip isolation were attained by the use of RIE(Reactive Ion Etching). Compared with the chemical wet etching, the RIE technique provides a potentially suprior means of etching substrates uniformly with reproducibility. Compound gases containing BCl_3 were chosen as the reactive etchant, because polymer remains on etched surface in the standard gases using CCl_2F_2. Fig.2 shows a SEM photograph of the cross section view in a deeply etched substrate. The typical etching temperature and time were about 70°C and 30 minutes for the 30 μm thick GaAs substrates. Since no significant side-etching occurs, the uniformity of the via holes is excellent, acrossa large-area wafer. This precise processing establishes uniform source inductance across the chip and between the chips. The RIE etching were performed using a photoresist mask in the via-hole process and using the gold-plated heat sink as a mask in the chip isolation process. In the PHS process, high speed gold plating, which utilizes solution flow through the plating cell, was applied to form the 50 μm thick metallization in short time. The plating rate was 0.6 minutes/μm. Fig.3 shows the backside view of a completed wafer with selective 50 μm thick metallization.

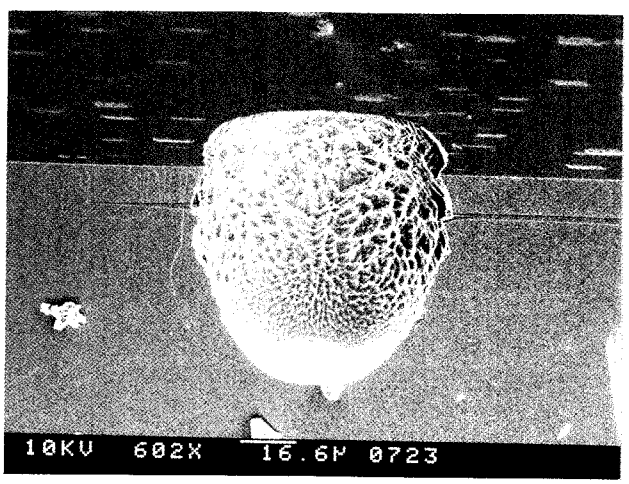

Fig.2 Cross section view of via hole

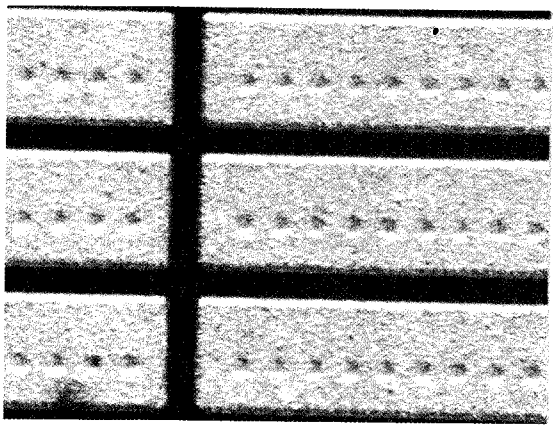

Fig.3 Backside view of a completed wafer after PHS metallization

INTERNAL MATCHING

The input and output internal matching circuits were both constructed with chip capacitors and distributed circuits for the X and Ku band devices. Fig.4 shows a top view of a Ku-band internally matched GaAs FET, consisting of two chips. The package size is 21mm × 12.9mm. The input and output circuits both consist of a 2-section LC low pass filter network, in which the inductor L is formed using bonding wires. The circuit elements for the X and Ku band devices were optimized by an in-house computor simulation program.

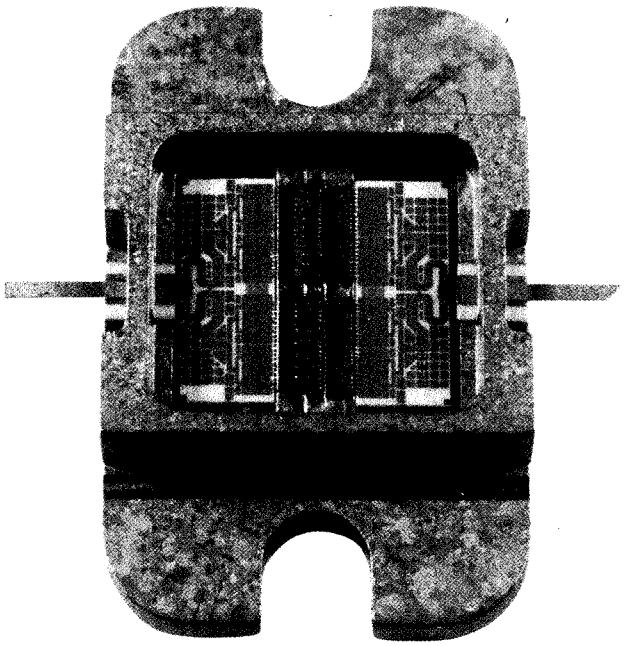

Fig.4 Ku band internally matched GaAs FET

In this study,an accurate wire bonding technique was investigated to minimize inductance variations related to differences in wire length and wire pitch. This technique involve the use of an automatic bonder and the newly designed FET chip. In the automatic bonder,the positions of wire bonds were programmed,keeping wire length and pitch constant for each lumped circuit. Furthermore,all of the bond positions on the FET chip could be arranged in conjunction with the locations of the input and output chip capacitors. This may be seen in a magnified inner view of an internally matched device,shown in Fig.5. This wire bonding technique permits mass production,by increasing the throughput and yield,and by lowering the labor costs.

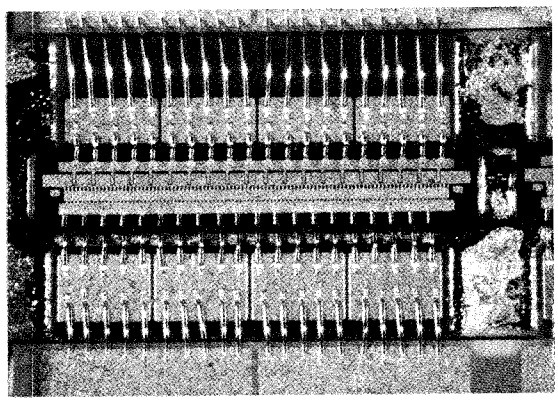

Fig.5 Magnified inner view of internally matched device

DC-RF PERFORMANCE

The saturated drain current(Idss) of a 16mm FET chip was set to about 4.0 A(0.25A/mm) to ensure a area of safety operation. The typical breakdown voltage between gate and source was measured to be -8V, when defined at the leakage current of 60 μA. The channel-to-case thermal resistance of the 2-chip device was about 1.2°C/W,measured by the IR method. The RF performance of the X and Ku band devices were tested under the bias condition of Vds=10V.

Fig.6 shows the output power(P_{out}) and the power added efficiency(η_{add}) versus the input power(P_{in}) for the X and Ku band devices,with additional tuning. At 11.2 GHz,the X band device achieved an output power(P_{1dB}) of 41.2 dBm(13W),a power gain(G_{1dB}) of 5.8 dB and a power added efficiency(η_{add}) of 25 % at the 1dB gain compression point. At 14.25 GHz,the Ku band device delivered the output power(P_{1dB}) of 41 dBm(12.6W) with 5 dB power gain(G_{1dB}) and 21 % power added efficiency(η_{add}). These results show state-of-the-art high power performance for X and Ku band power GaAs FETs.

Fig.7 and 8 show the P_{1dB} and linear power gain(G_{LP}) characteristics of the X and Ku band devices,in the 10.7-11.7 GHz and 14.0-14.5 GHz bands. Typical output powers of more than 10W were obtained for both devices,with no additional tuning.

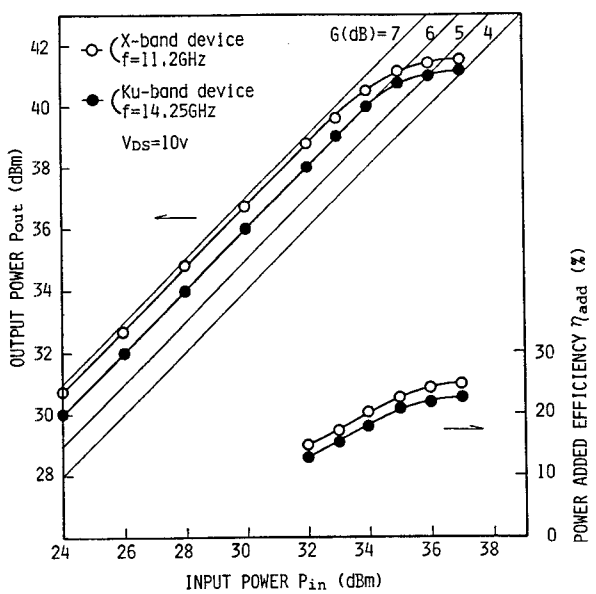

Fig.6 Output power and power added efficiency versus input power for X and Ku band devices

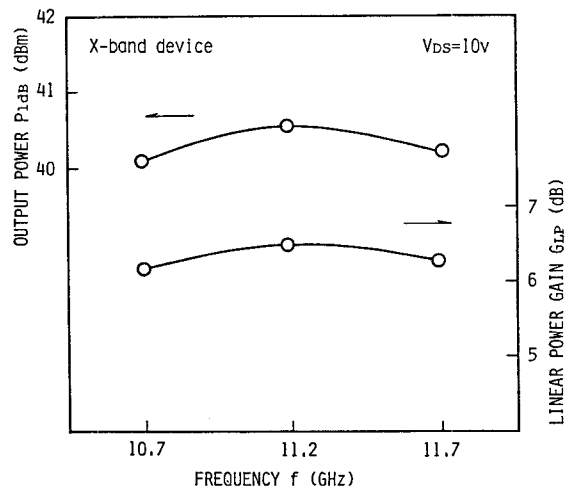

Fig.7 Output power and linear power gain versus frequency for X band device

Fig.9 shows the third order intermodulation characteristics of the Ku band device, by the two tone test. An IM of 40 dBc was obtained at the output power of 34 dBm(6 dB back-off point from 40 dBm),and the intercept point was 53 dBm. These results are sufficient for digital communication system applications.

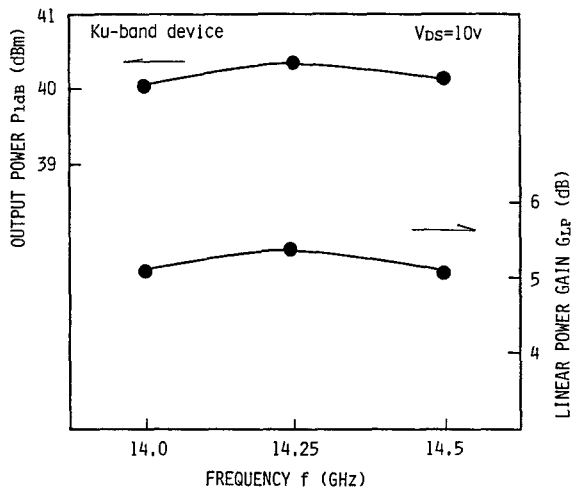

Fig.8 Output power and linear power gain versus frequency for Ku band device

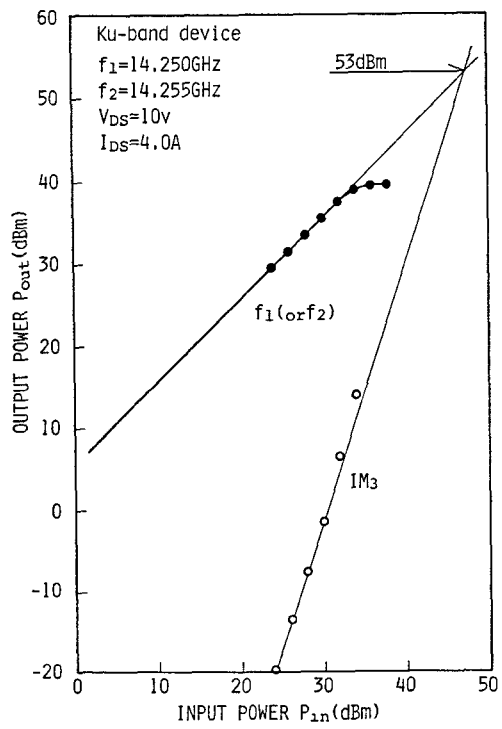

Fig.9 Third order intermodulation characteristics of Ku band device

COCLUSION

Power GaAs FETs,with state-of-the-art high power performance,have been developed that deliver output powers of more than 10W for the X and Ku bands. At the band center frequency of 11.2 GHz,an output power(P_{1dB}) of 13W with 5.8 dB gain and 25 % power added efficiency was obtained. At 14.25 GHz, P_{1dB}, G_{1dB} and η_{add} were 12.6W,5 dB and 21 % respectively. These performance results are due to the chip uniformity and the combined effect of the internal matching circuit. The present techniques,which are the direct ion implantation,the reactive ion etching and the use of an automatic bonder,are highly reproducible on mass-production basis, and will promize the approach to higher power multichip device.

ACKNOWLEDGEMENT

The authors wish to thank S.Okano, K.Mishima,K.Kamei and M.Higashiura for their encouragement and helpful discussions, and S.Yanagawa and T.Yoshida for valuable contributions through this work.

REFERENCES

(1) S.Yanagawa,Y.Yamada,M.Itoh,K.Arai and N.Tomita, HIGH EFFICIENCY ION-IMPLANTED POWER GaAs FETs FOR C AND X BANDs,"IEEE MTT-S Digest,pp332-335,June 1985

(2) M.Avasarala and D.S.Day, 2.5-WATT AND 5-WATT INTERNALLY MATCHED GaAs FETs FOR 10.7-11.7 AND 14-14.5 GHz BANDs," IEEE MTT-S Digest,pp455-458,June 1986

(3) Y.Kadowaki,S.Igi,M.Wataze,T.Sonoda, K.Hayashi,M.Yamanouchi,S.Takamiya and S.Mitsui, A 6 WATT POWER GaAs FET FOR 14.0-14.5 GHz BAND,"IEEE MTT-S Digest, pp845-847,June 1987